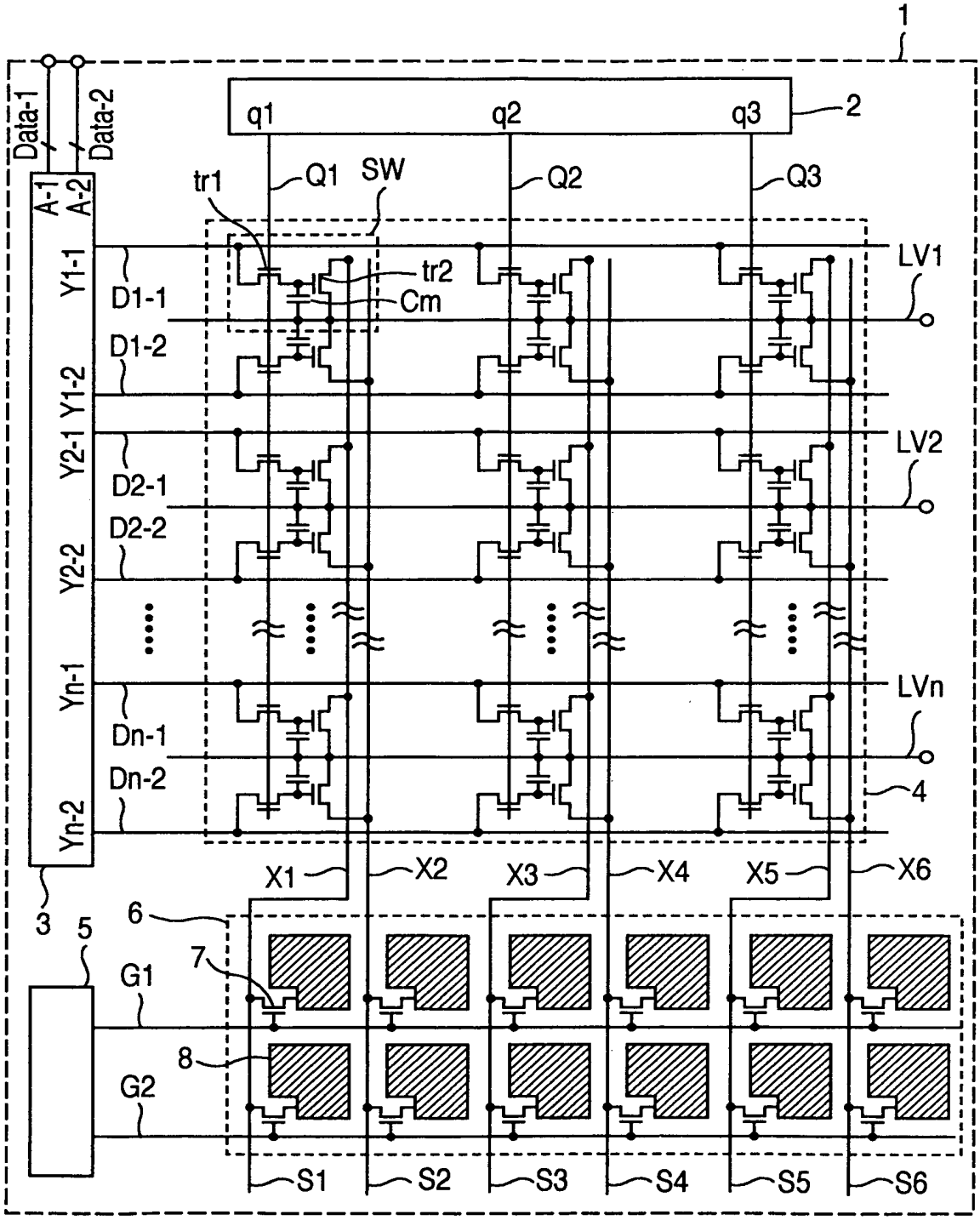
FIG.1



1 : INSULATING SUBSTRATE
2 : SHIFT REGISTER
3 : DECODER
4 : DA CONVERTER
5 : SCANNING CIRCUIT
6 : DISPLAY REGION
7 : PIXEL TFT
8 : PIXEL
SW : SWITCH CIRCUIT

FIG.2

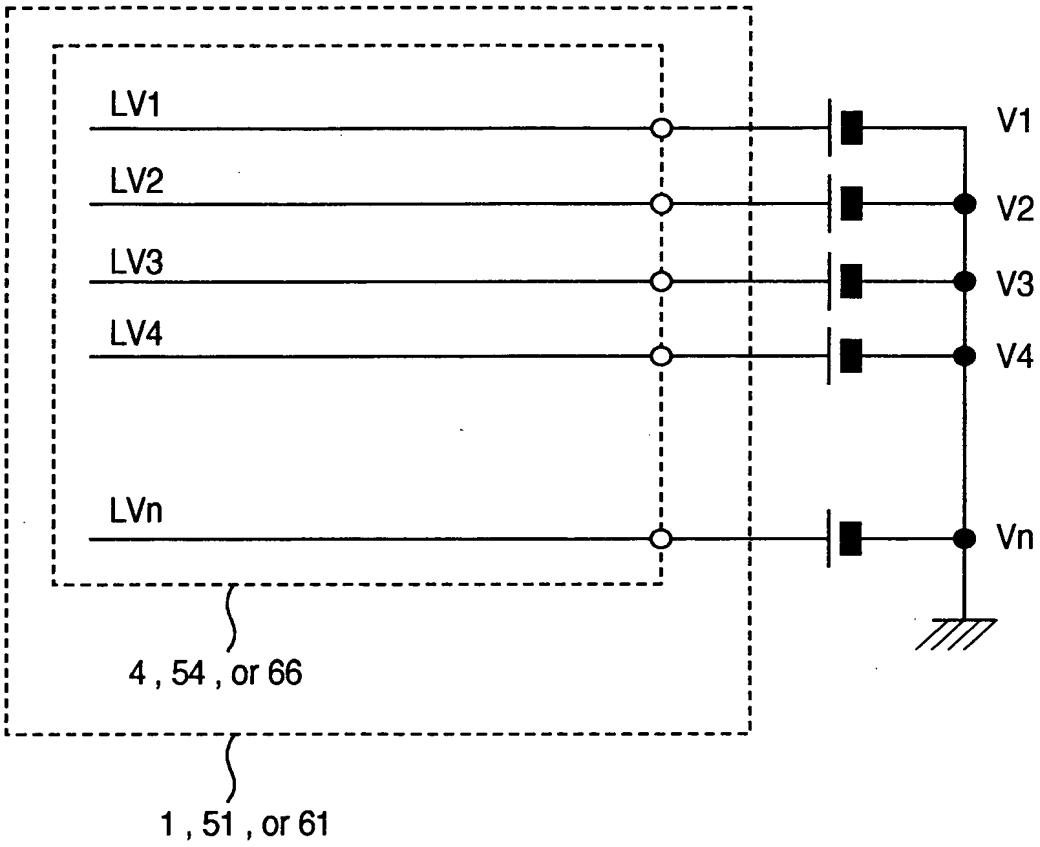


FIG.3

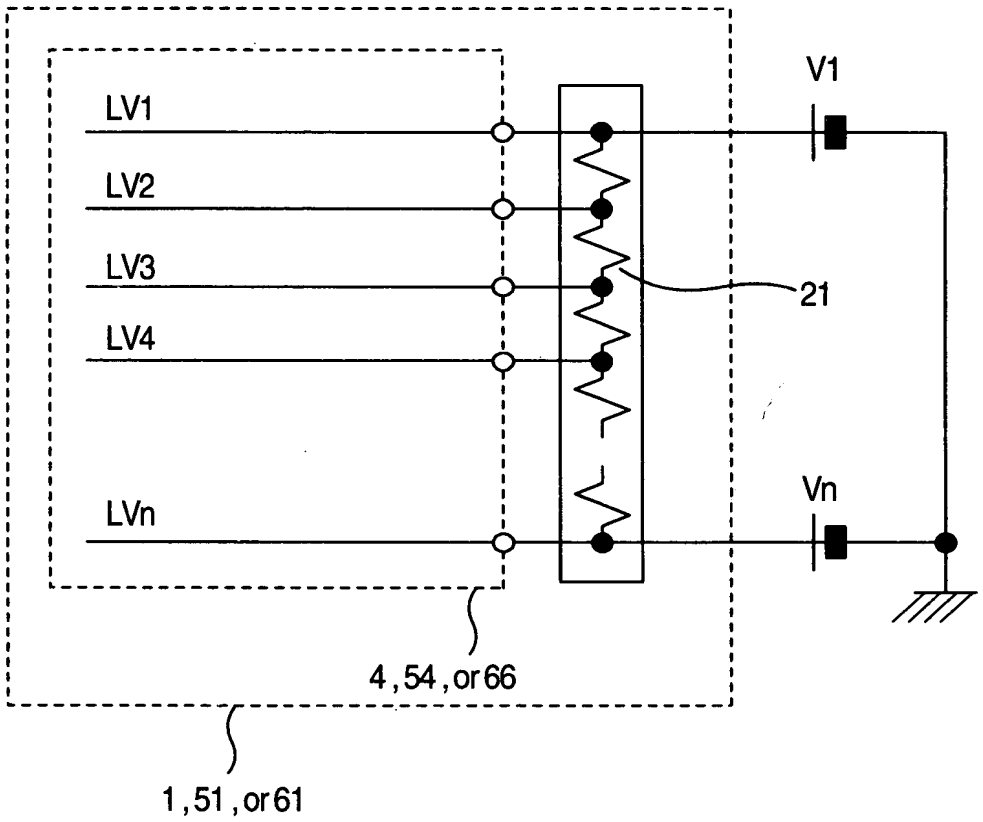


FIG.4

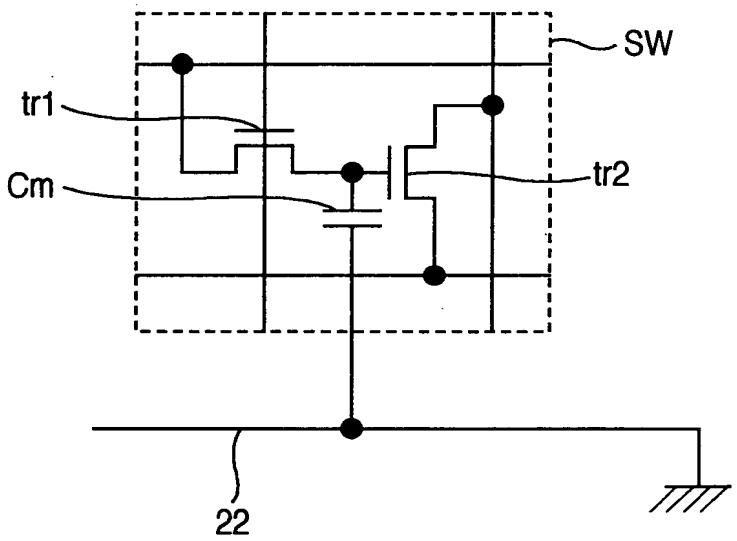


FIG.5

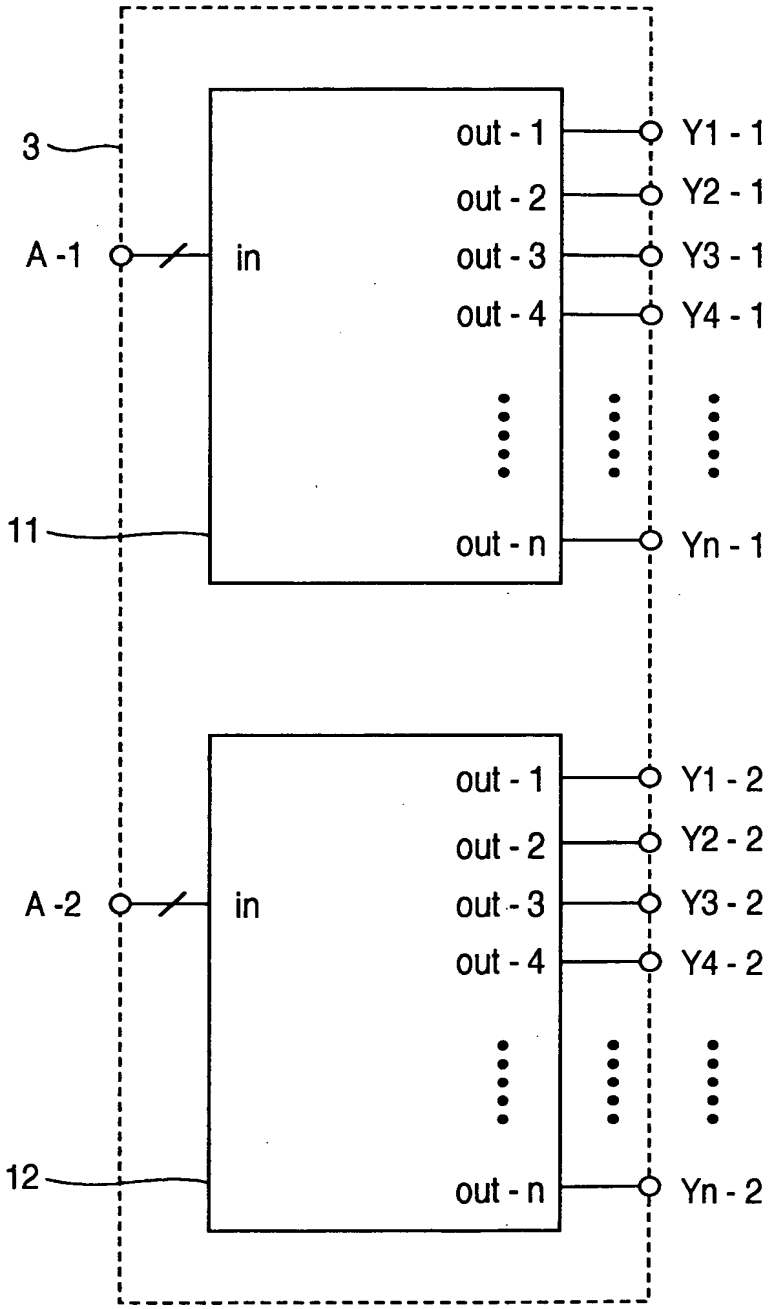

3
A -1
in
out - 1
out - 2
out - 3
out - 4
Y1 - 1
Y2 - 1
Y3 - 1
Y4 - 1
11
out - n
Yn - 1
A -2
in
out - 1
out - 2
out - 3
out - 4
Y1 - 2
Y2 - 2
Y3 - 2
Y4 - 2
12
out - n
Yn - 2

FIG.6

in	out - 1	out - 2	out - 3	out - 4	out - 5	.....	out - n
1	1	0	0	0	0	.....	0
2	0	1	0	0	0	.....	0
3	0	0	1	0	0	.....	0
4	0	0	0	1	0	.....	0
5	0	0	0	0	1	.....	0
⋮	⋮	⋮	⋮	⋮	⋮	⋱	⋮
n	0	0	0	0	0	.....	1

FIG.7

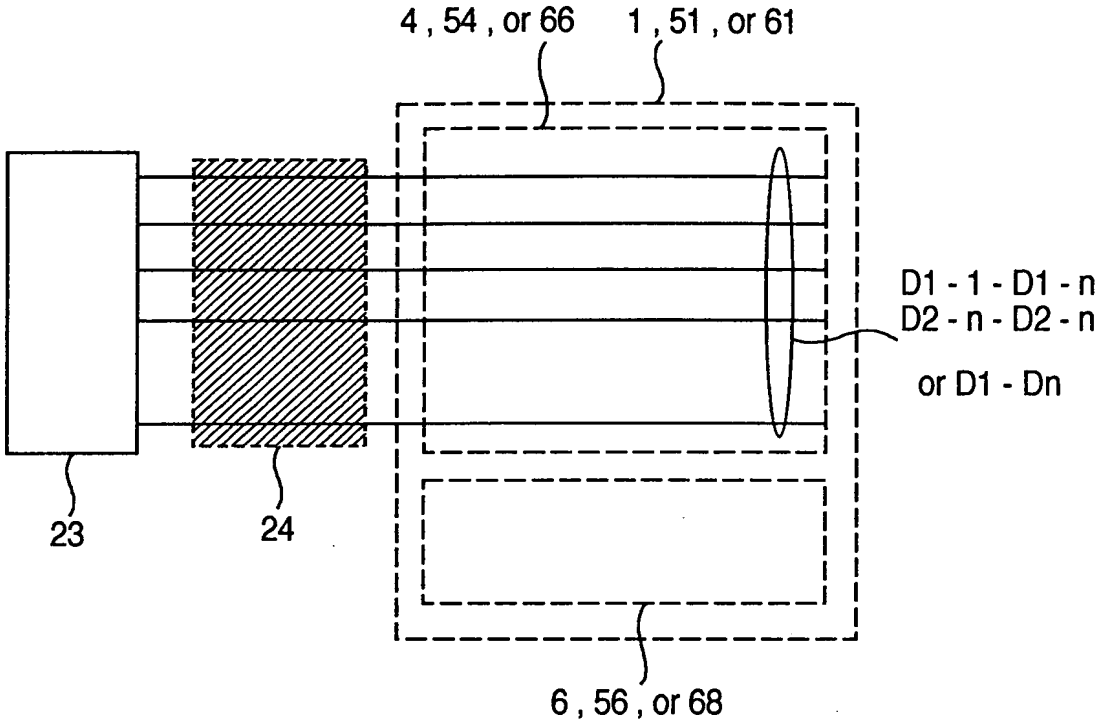

4 , 54 , or 66
1 , 51 , or 61
D1 - 1 - D1 - n
D2 - n - D2 - n
or D1 - Dn
23
24
6 , 56 , or 68

FIG.8

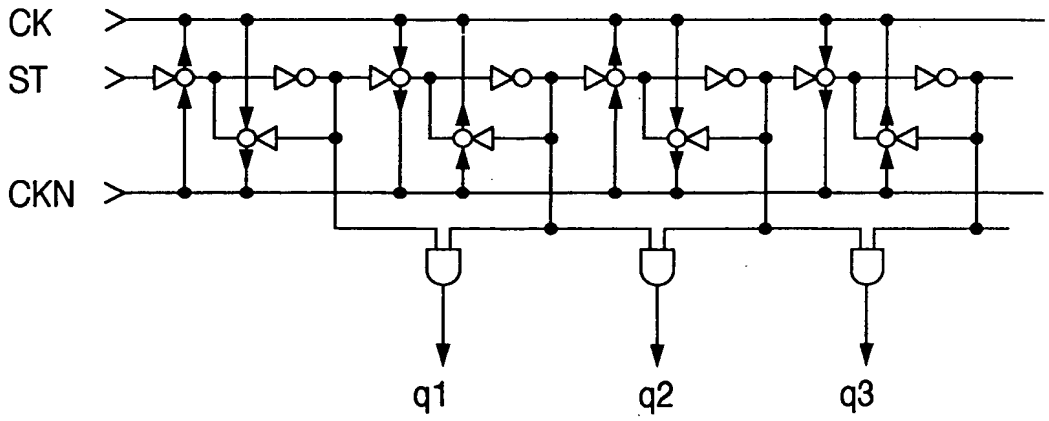

CK
ST
CKN
q1
q2
q3

FIG.9A

INVERTER

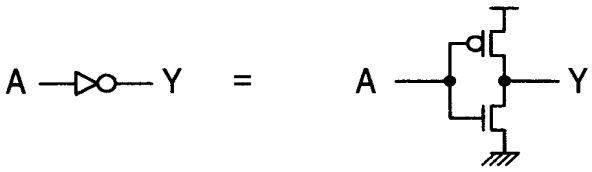


FIG.9B

CLOCKED INVERTER

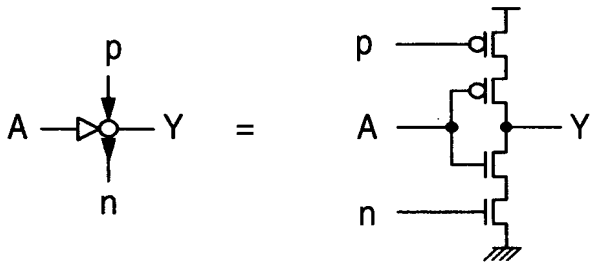


FIG.9C

AND GATE

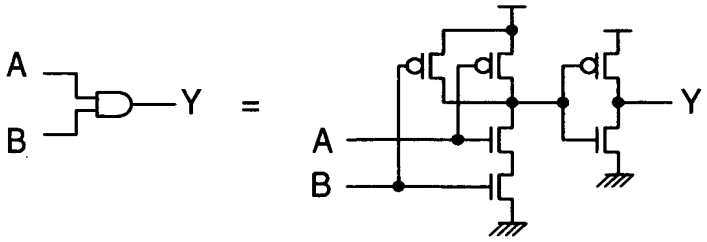


FIG.10

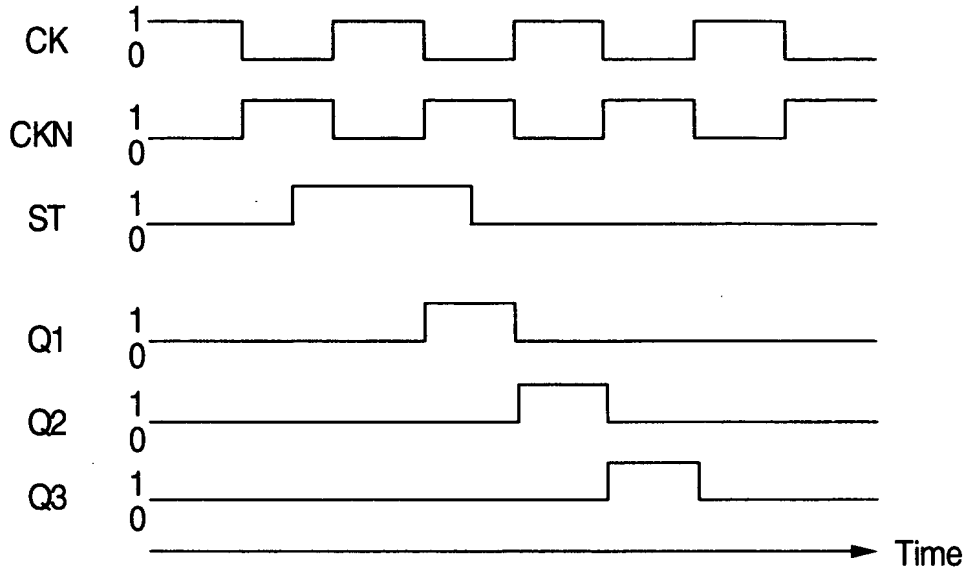


FIG.11

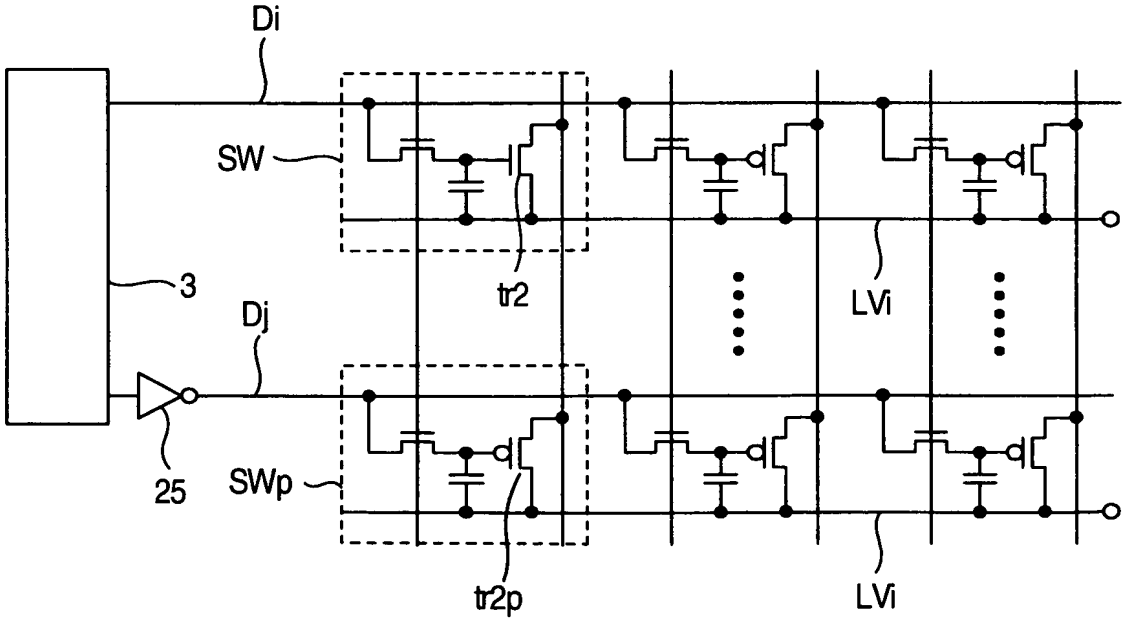


FIG.12

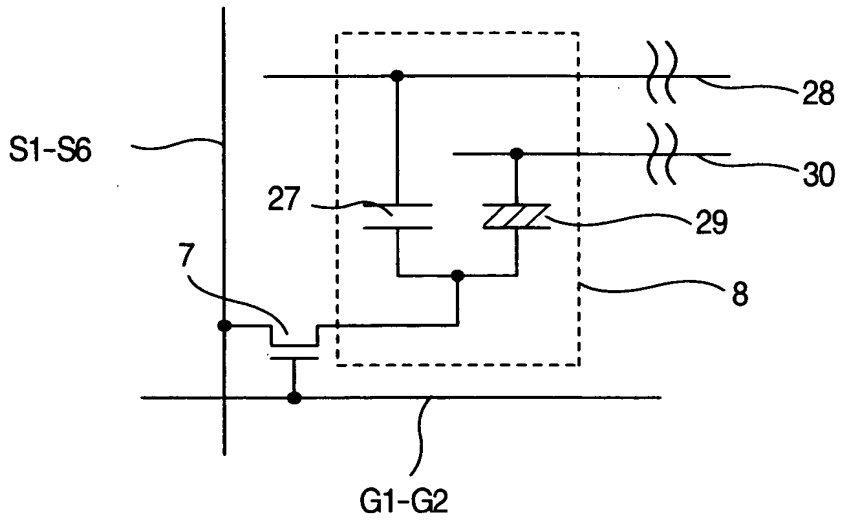


FIG.13

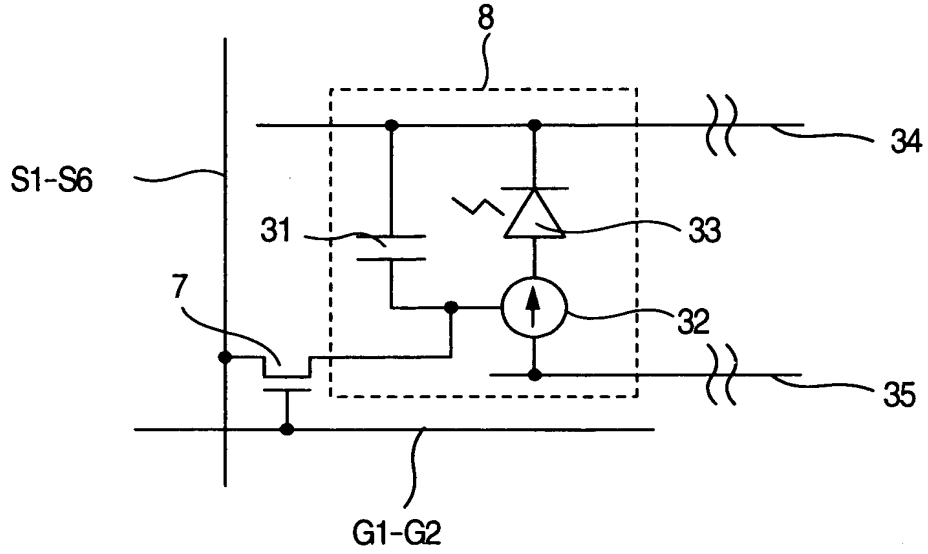


FIG.14

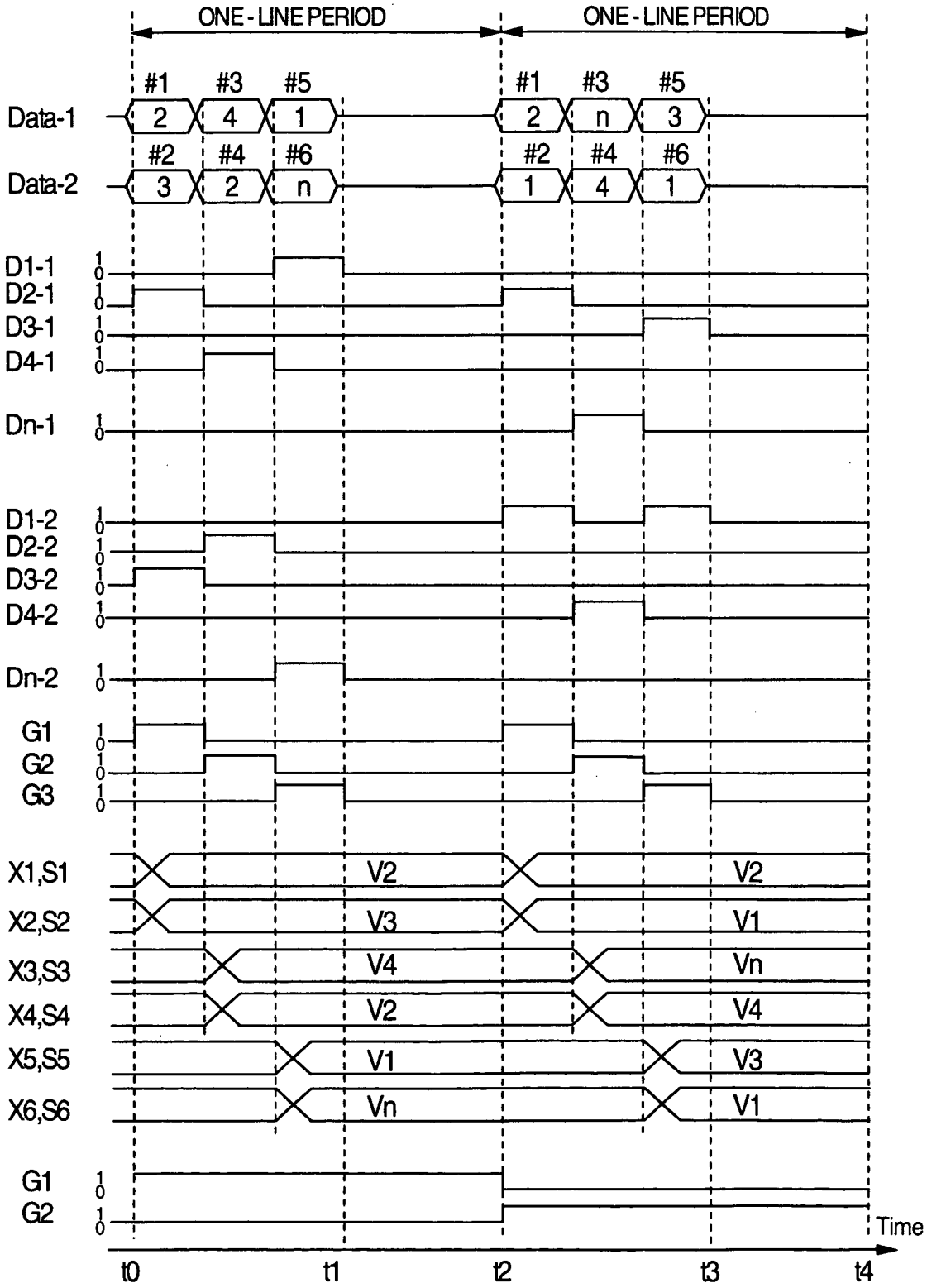

ONE - LINE PERIOD
ONE - LINE PERIOD
#1
#3
#5
#1
#3
#5
Data-1
2
4
1
2
n
3
#2
#4
#6
#2
#4
#6
Data-2
3
2
n
1
4
1
D1-1
D2-1
D3-1
D4-1
Dn-1
D1-2
D2-2
D3-2
D4-2
Dn-2
G1
G2
G3
X1,S1
X2,S2
X3,S3
X4,S4
X5,S5
X6,S6
V2
V3
V4
V2
V1
Vn
V2
V4
V1
V3
Vn
V1
G1
G2
Time
t0
t1
t2
t3
t4

FIG.15

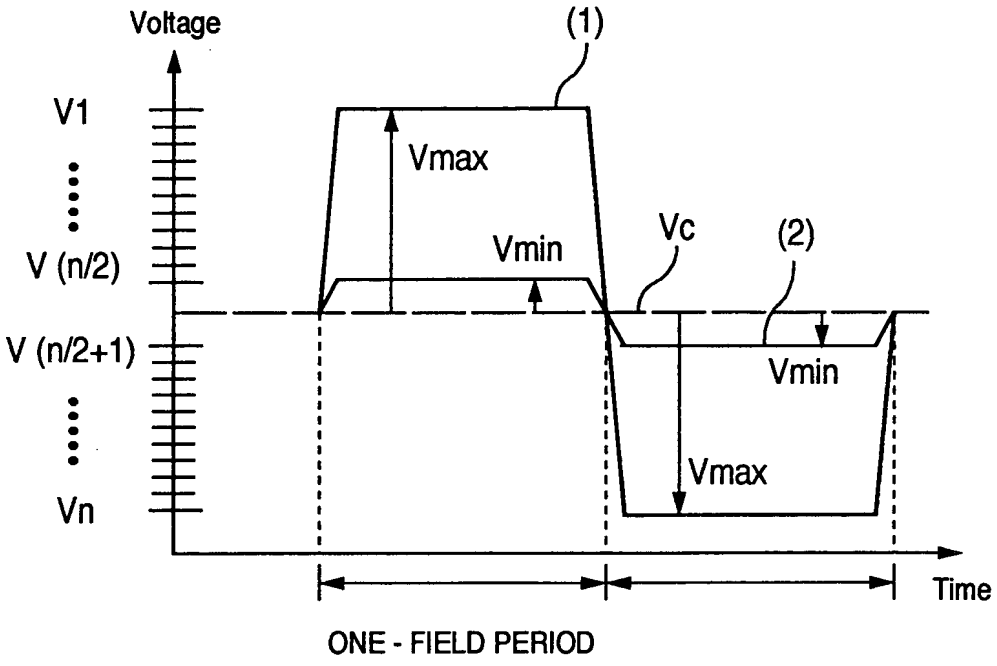

Voltage
(1)
V1
Vmax
Vmin
Vc
(2)
V (n/2)
V (n/2+1)
Vmin
Vmax
Vn
Time
ONE - FIELD PERIOD

FIG.16

	in	out - 1	out - 2	out - 3	.....	out - n	out - (n/2+1)	.....	out - (n-2)	out - (n-1)	out - n
Odd	1	1	0	0	.....	0	All 0				
	2	0	1	0	.....	0					
	3	0	0	1	.....	0					
	⋮	⋮	⋮	⋮	⋱	⋮					
	n/2	0	0	0	.....	1					
Even	1	All 0					0	.....	0	0	1
	2						0	.....	0	1	0
	3						0	.....	1	0	0
	⋮						⋮	⋱	⋮	⋮	⋮
	n/2						1	.....	0	0	0

FIG.17

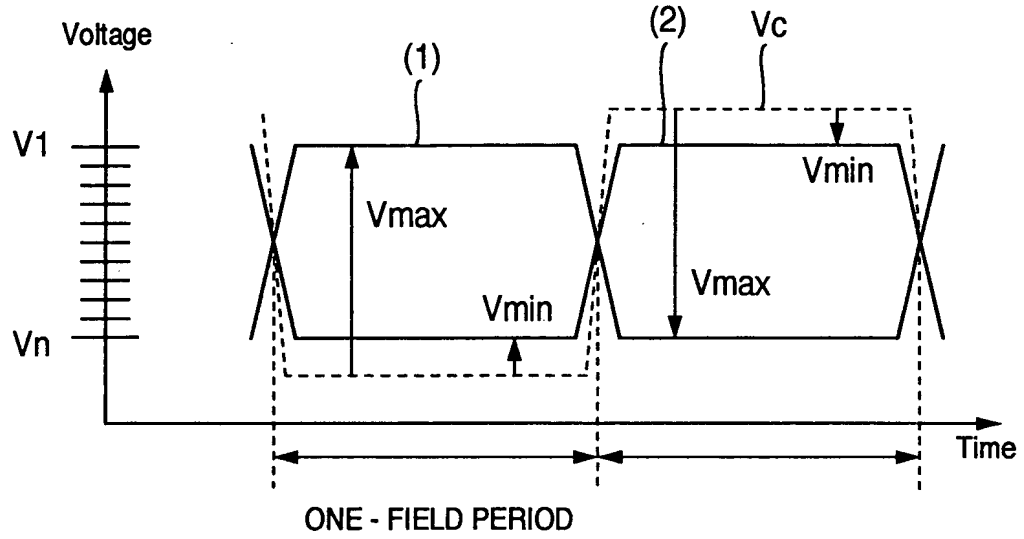


FIG.18

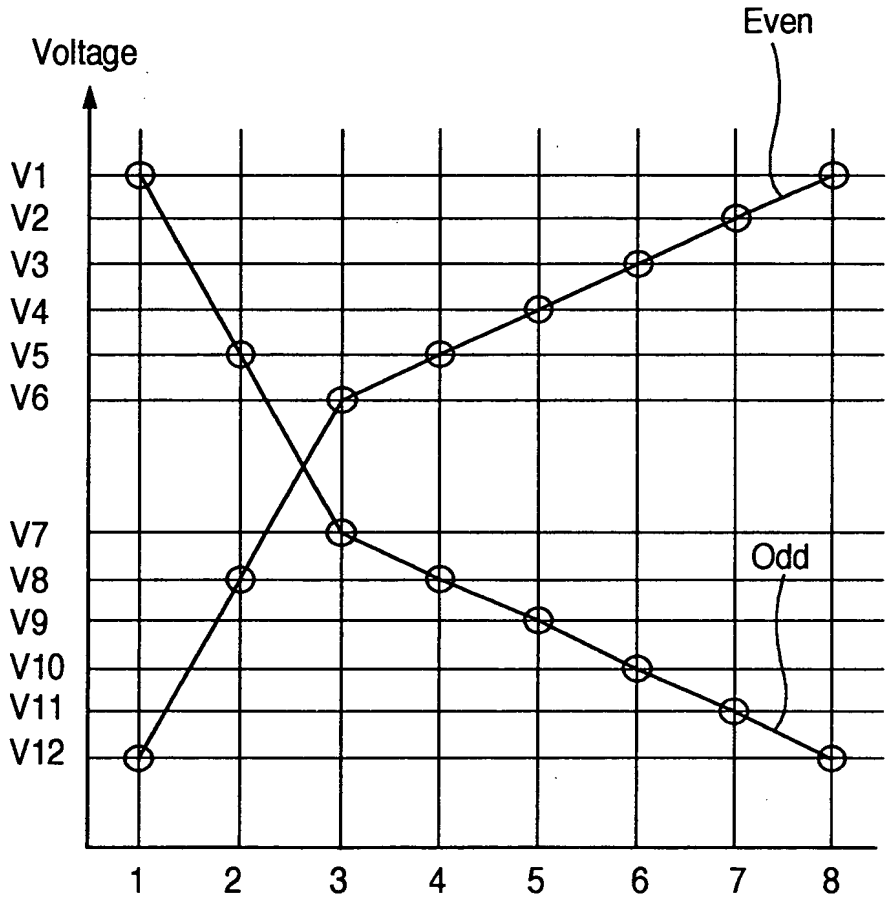
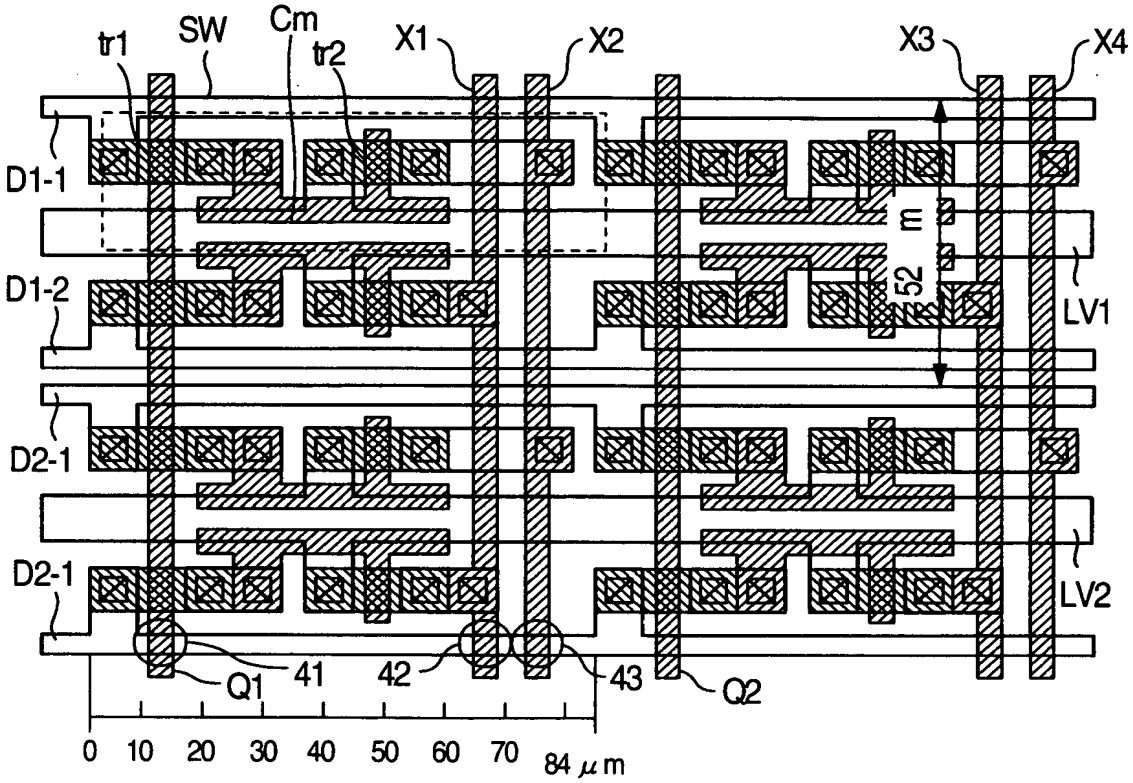


FIG.19

	in	out-1	out-2	out-3	out-4	out-5	out-6	out-7	out-8	out-9	out-10	out-11	out-12
Odd	1	1	0	0	0	0	0	0	0	0	0	0	0
	2	0	0	0	0	1	0	0	0	0	0	0	0
	3	0	0	0	0	0	0	1	0	0	0	0	0
	4	0	0	0	0	0	0	0	1	0	0	0	0
	5	0	0	0	0	0	0	0	0	1	0	0	0
	6	0	0	0	0	0	0	0	0	0	1	0	0
	7	0	0	0	0	0	0	0	0	0	0	1	0
	8	0	0	0	0	0	0	0	0	0	0	0	1
Even	1	0	0	0	0	0	0	0	0	0	0	0	1
	2	0	0	0	0	0	0	0	1	0	0	0	0
	3	0	0	0	0	0	1	0	0	0	0	0	0
	4	0	0	0	0	1	0	0	0	0	0	0	0
	5	0	0	0	1	0	0	0	0	0	0	0	0
	6	0	0	1	0	0	0	0	0	0	0	0	0
	7	0	1	0	0	0	0	0	0	0	0	0	0
	8	1	0	0	0	0	0	0	0	0	0	0	0

FIG.20



EXAMPLE

INTERSECTION OF GATE METAL FILM AND POLYSILICON FILM

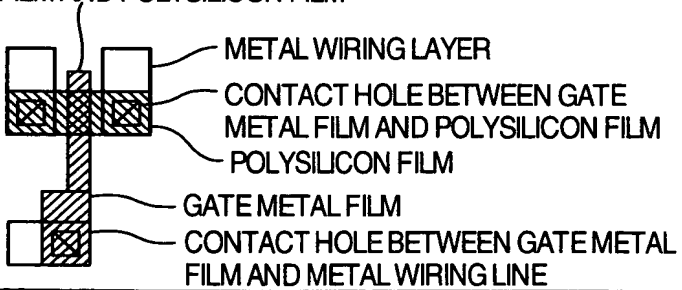


FIG.21

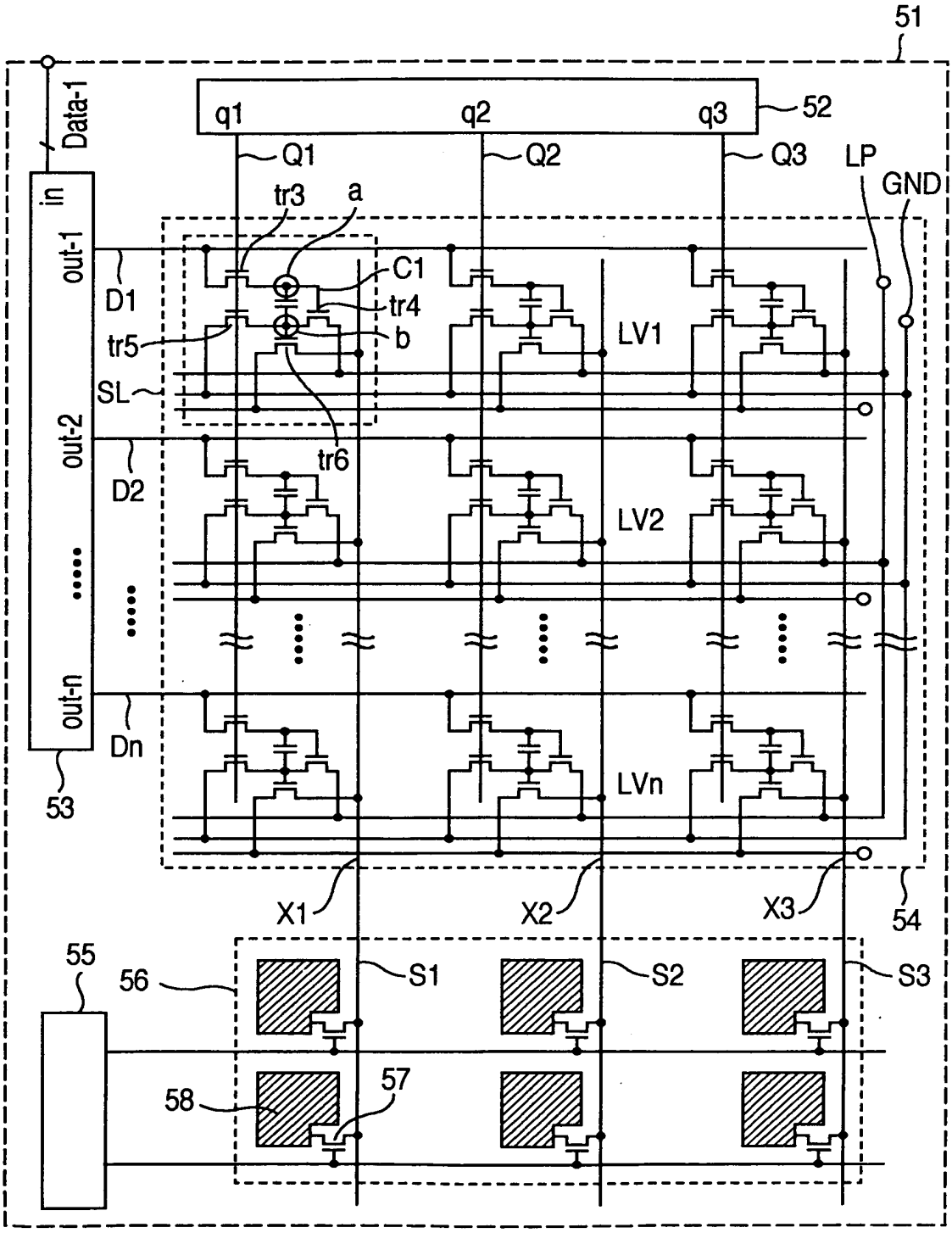

51
Data-1
in
out-1
out-2
out-n
53
q1
q2
q3
52
Q1
Q2
Q3
LP
GND
tr3
a
C1
tr4
b
tr5
tr6
D1
D2
Dn
SL
LV1
LV2
LVn
X1
X2
X3
54
55
56
S1
S2
S3
57
58

FIG.22

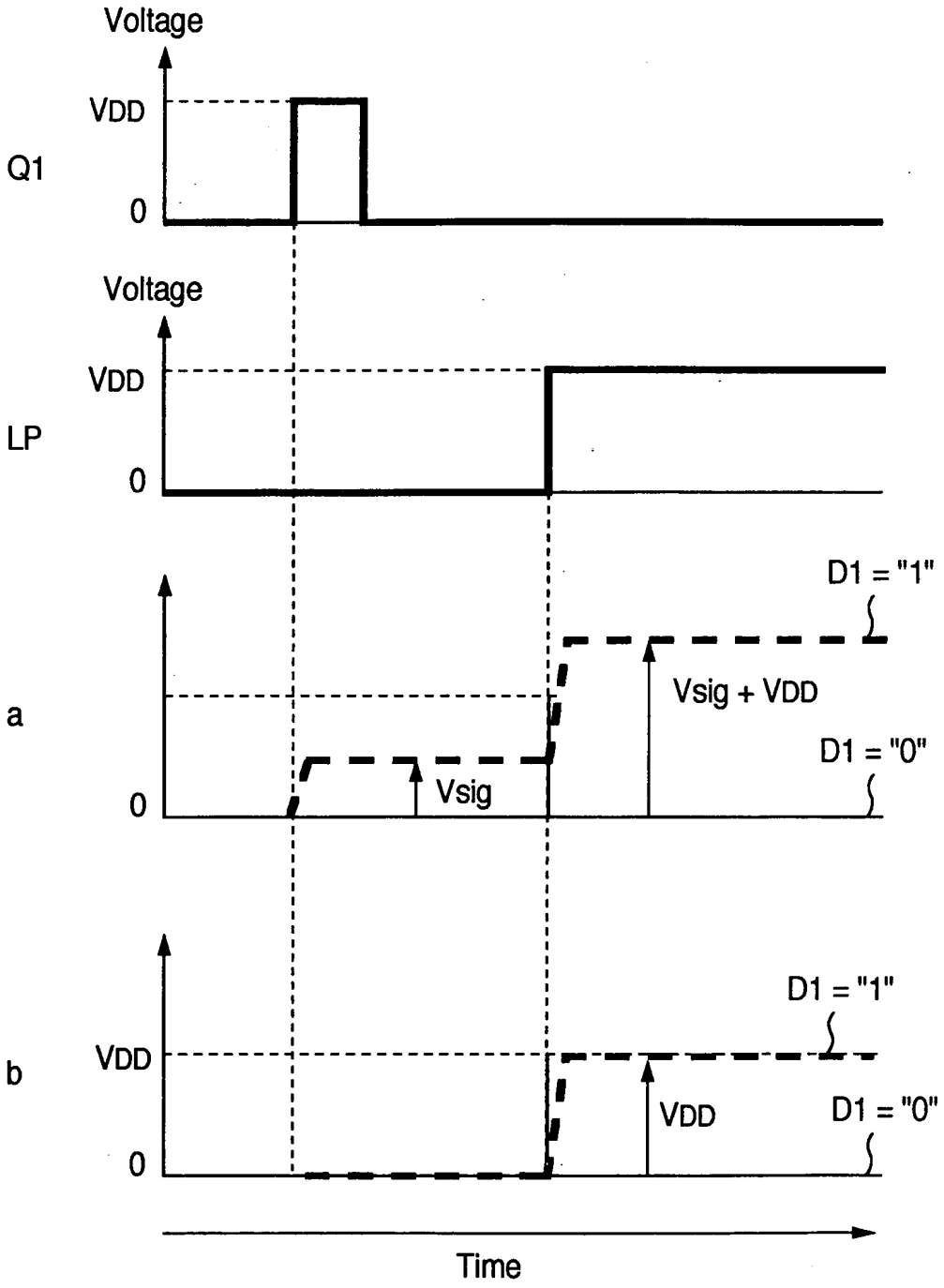

Voltage
VDD
Q1
0
Voltage
VDD
LP
0
D1 = "1"
Vsig + VDD
a
D1 = "0"
Vsig
0
D1 = "1"
VDD
b
VDD
D1 = "0"
0
Time

FIG.23

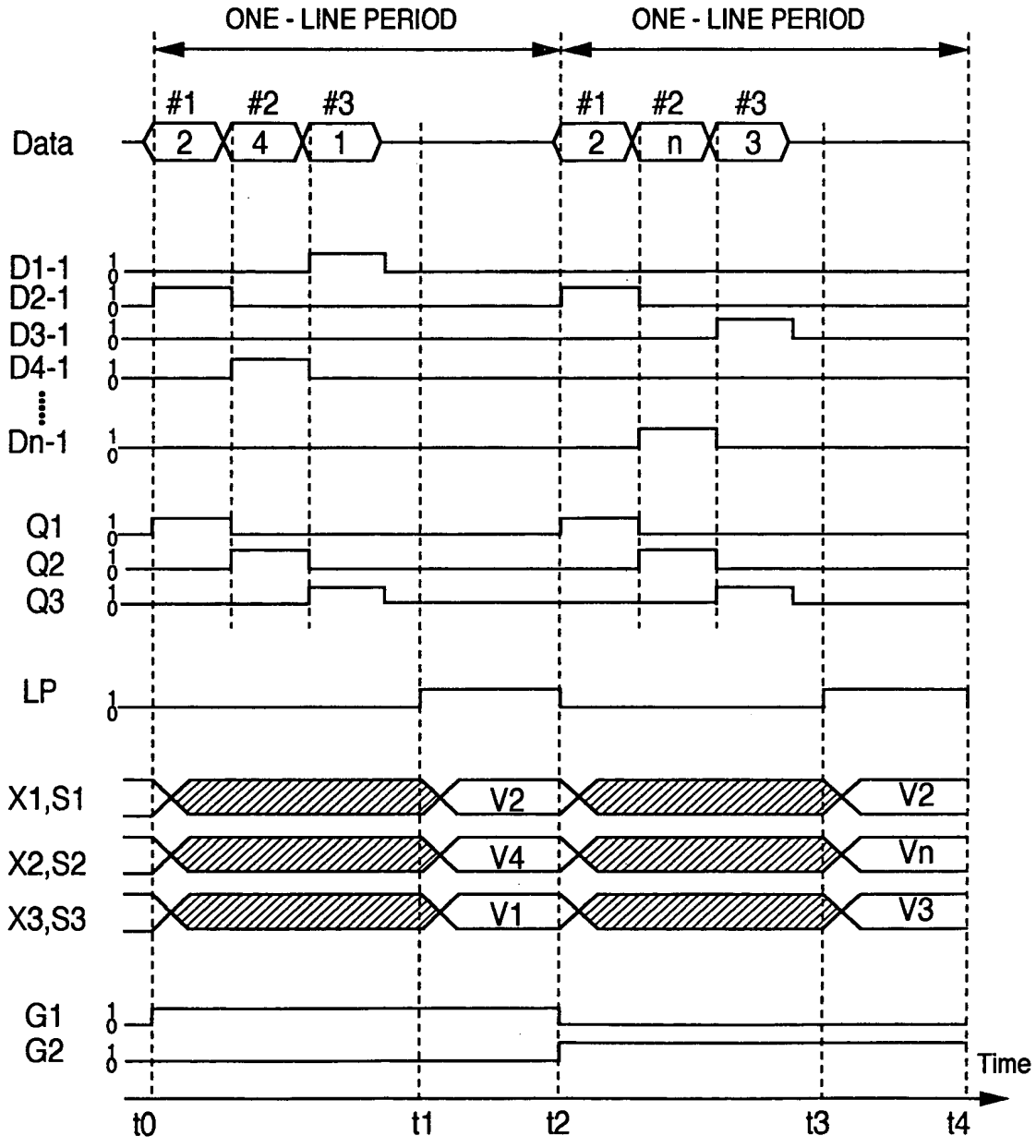

ONE - LINE PERIOD
ONE - LINE PERIOD
#1
#2
#3
#1
#2
#3
Data
2
4
1
2
n
3
D1-1
D2-1
D3-1
D4-1
Dn-1
Q1
Q2
Q3
LP
X1,S1
X2,S2
X3,S3
V2
V4
V1
V2
Vn
V3
G1
G2
Time
t0
t1
t2
t3
t4

FIG.24

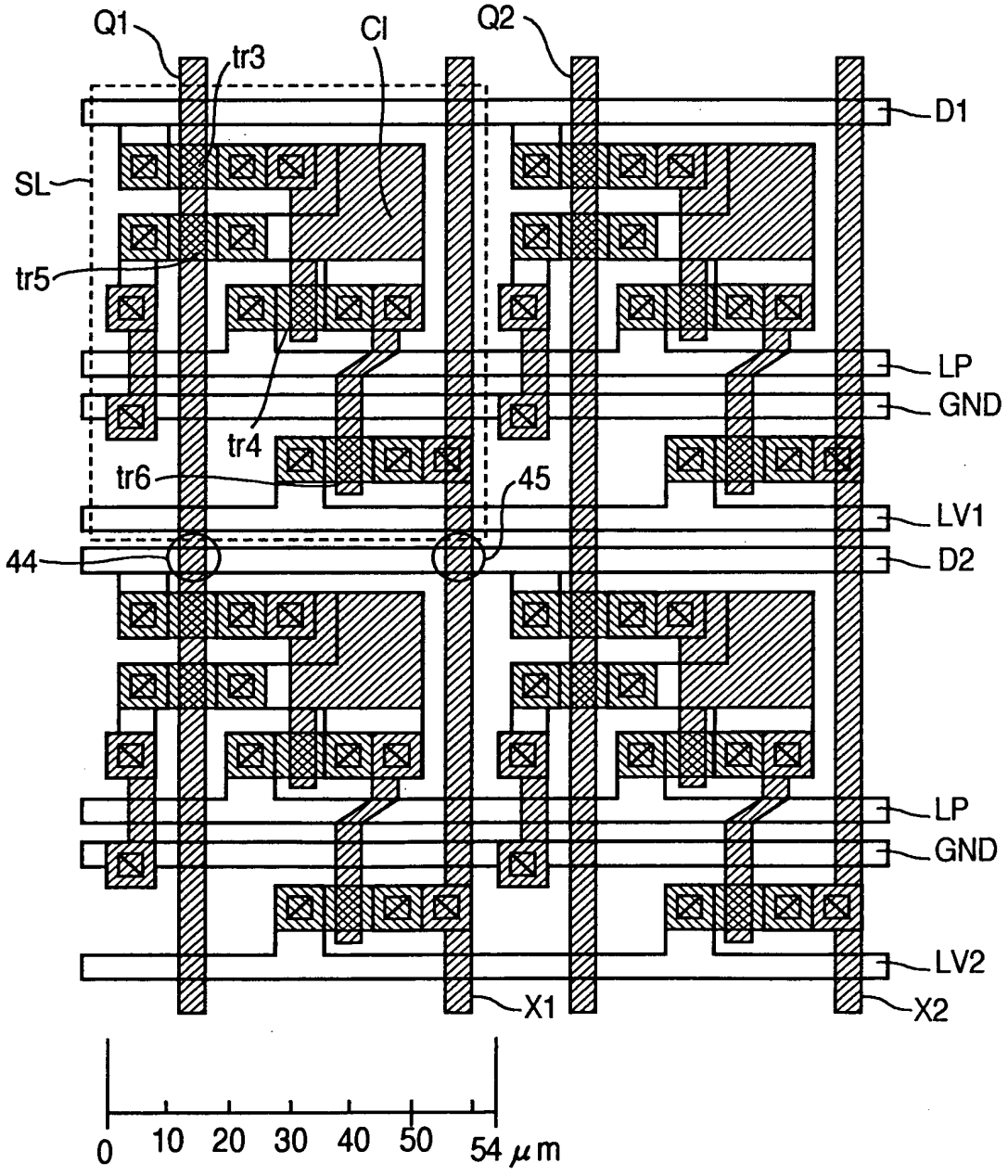

Q1
tr3
Cl
Q2
D1
SL
tr5
LP
GND
tr4
tr6
45
LV1
44
D2
LP
GND
LV2
X1
X2
0
10
20
30
40
50
54 μm

FIG.25

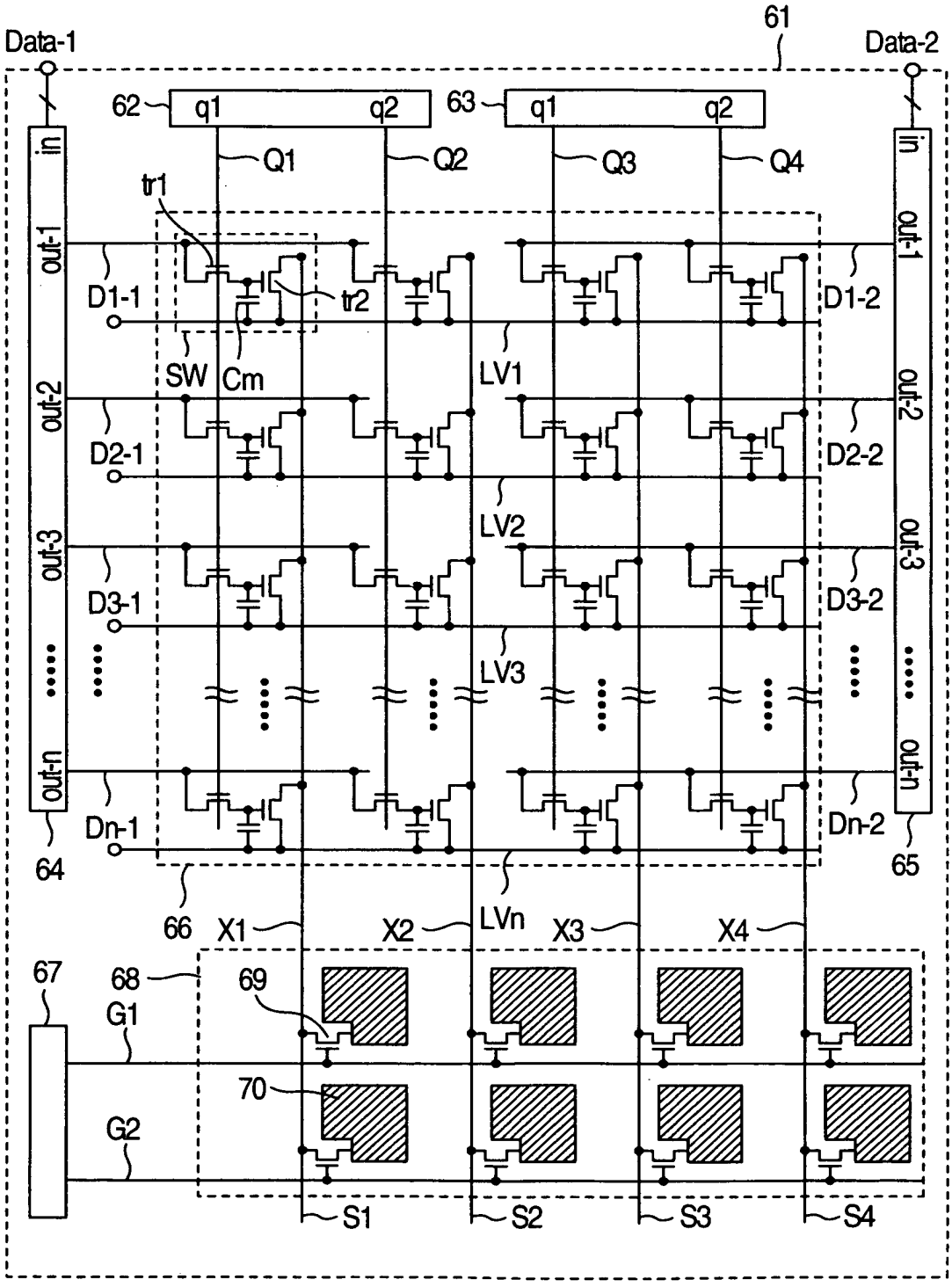

61
Data-1
Data-2
62
63
q1
q2
Q1
Q2
Q3
Q4
tr1
tr2
in
out-1
out-2
out-3
out-n
D1-1
D2-1
D3-1
Dn-1
D1-2
D2-2
D3-2
Dn-2
SW
Cm
LV1
LV2
LV3
LVn
64
65
66
X1
X2
X3
X4
67
68
69
70
G1
G2
S1
S2
S3
S4

FIG.26

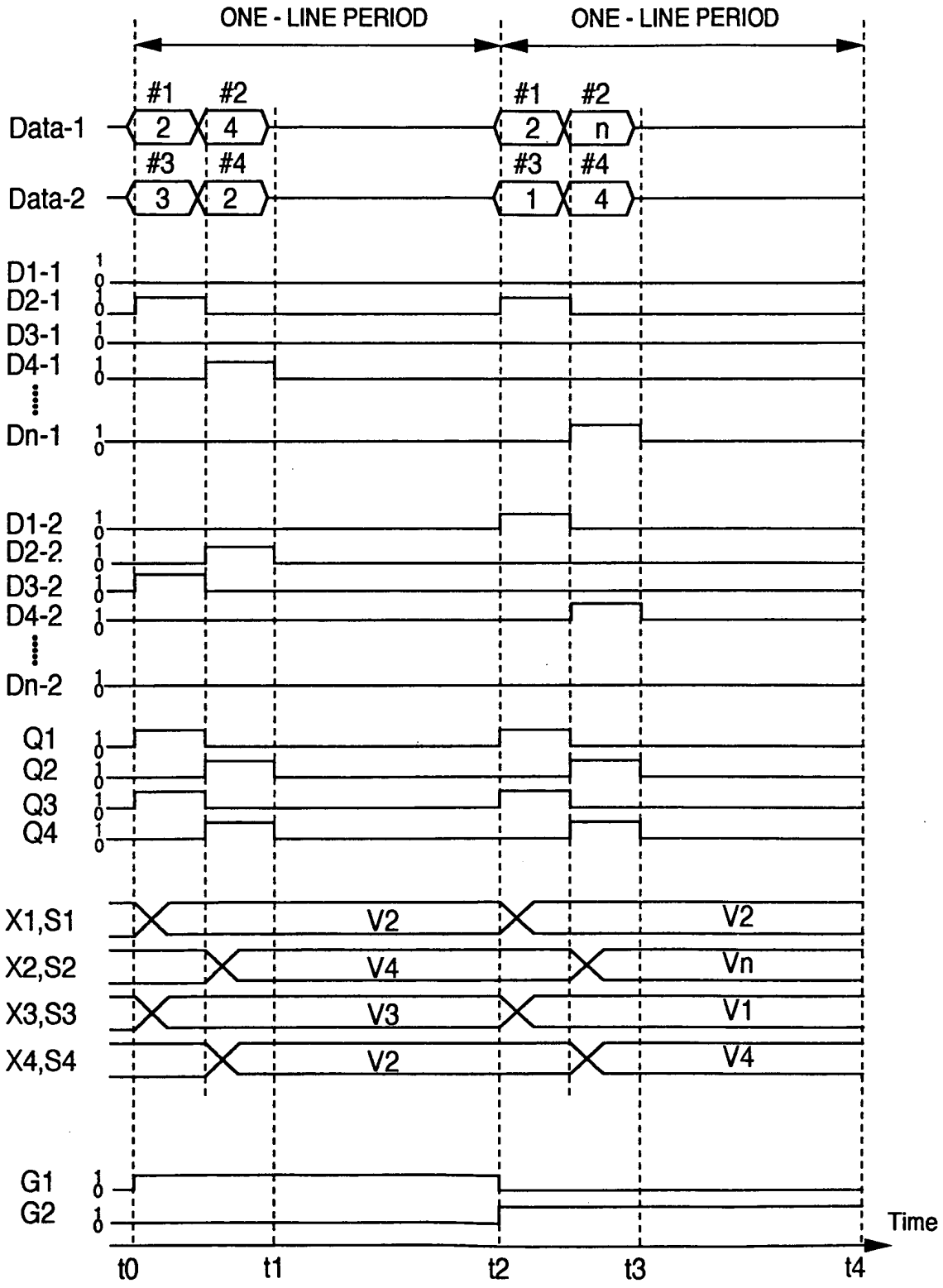

ONE - LINE PERIOD
ONE - LINE PERIOD
#1
#2
#1
#2
Data-1
2
4
2
n
#3
#4
#3
#4
Data-2
3
2
1
4
D1-1
D2-1
D3-1
D4-1
Dn-1
D1-2
D2-2
D3-2
D4-2
Dn-2
Q1
Q2
Q3
Q4
X1,S1
V2
V2
X2,S2
V4
Vn
X3,S3
V3
V1
X4,S4
V2
V4
G1
G2
Time
t0
t1
t2
t3
t4

FIG.27